What is claimed is:
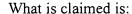
1.   A method for minimizing nth-order harmonic associated with a square wave clock signal having a predetermined frequency and a duty cycle, comprising:

changing the duty cycle of the clock to eliminate or suppress the nth-order

5   harmonic of the clock; and

generating a low-interference clock having the changed duty cycle while keeping the predetermined frequency.

2.   The method of claim 1, wherein generating a low-interference clock further

10 comprises generating an asymmetrical clock signal.

3.   The method of claim 1, wherein the square wave clock has rising and falling edges and wherein changing the duty cycle further comprises changing the position of the falling edge of the square wave clock relative to the position of the rising edge of the

15 clock.

4.   The method of claim 1, wherein minimizing the nth-order harmonic changes the magnitude of other harmonic.

20 5.   The method of claim 1, further comprising applying the clock in a digital receiver.

6.   A system for minimizing nth-order harmonic associated with a square wave clock signal having a predetermined frequency and a duty cycle, comprising:

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means for changing the duty cycle of the clock to eliminate or suppress the nth-order harmonic of the clock; and
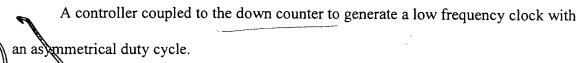
means for generating a low-interference clock having the changed duty cycle while keeping the predetermined frequency.

7.   The system of claim 6, wherein the means for generating a low-interference clock further comprises means for generating an asymmetrical clock signal.

8.   The system of claim 6, wherein the square wave clock has rising and falling edges
10 and wherein the means for changing the duty cycle further comprises means for changing the position of the falling edge of the square wave clock relative to the position of the rising edge of the clock.

9.   The system of claim 6, wherein minimizing the nth-order harmonic changes the
15 magnitude of other harmonic.

10.   The system of claim 6, wherein the low-interference clock is used in an intermediate frequency (IF) stage of a radio transceiver.

20   11. A clock generator, comprising:

A high frequency clock/oscillator;

A counter coupled to the clock/oscillator; and

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A controller coupled to the down counter to generate a low frequency clock with an asymmetrical duty cycle.

12. The clock generator of claim 11, wherein the clock oscillator generates an output at a high frequency relative to the low frequency clock.

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13. The clock generator of claim 11, wherein the counter is a down counter.

14. The clock generator of claim 11, wherein the counter is a modulo counter.

15. The clock generator of claim 11, wherein the symmetrical clock has rising and falling edges and wherein the controller changes the position of the falling edge of the symmetrical clock relative to the position of the rising edge of the

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symmetrical clock.

16. The clock generator of claim 11, wherein the controller minimizes the nth-order harmonic and changes the magnitude of other harmonic.

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